

Computer Architecture Section 80

CS 147

Fall 2023 3 Unit(s) 08/21/2023 to 12/06/2023 Modified 08/22/2023

Contact Information

Instructor(s):	Dr. Chung-Wen (Albert) Tsao
Office Location:	MH411
Email:	chung-wen.tsao@sjsu.edu (Once the class starts, use Canvas Inbox)
Class Days/Time:	T/R 1:30PM - 2:45PM
Classroom:	Join URL: https://sjsu.zoom.us/j/88921080354
<u>Office Hours:</u>	<ul style="list-style-type: none">• M/W 3 – 4 pm in office MH411• M/T/W/Th/F 3 – 4 pm on ZOOM<ul style="list-style-type: none">◦ Join URL: https://sjsu.zoom.us/j/86250414128 (https://sjsu.zoom.us/j/86250414128)
<u>Prerequisites:</u>	CS 47 or CMPE 102 or equivalent (with a grade of "C-" or better)
Class Meeting Dates	Aug 21, 2023 – Dec 6, 2023

Course Description and Requisites

Introduction to the basic concepts of computer hardware structure and design, including processors and arithmetic logic units, pipelining, and memory hierarchy.

Prerequisite(s): CS 47 or CMPE 102 (with a grade of "C-" or better), Computer Science, Applied and Computational Math, Forensic Science: Digital Evidence, or Software Engineering majors only; or instructor consent.

Letter Graded

Classroom Protocols

- Instructor may drop students (by the Instructor Drop Deadline) who
 - are absent for 1st day of class without informing you before 2nd day of class, or
 - have no proof of the prerequisite fulfillments.

- Do not ask for special treatment. The rules for this course apply to everyone equally.
- Cheating will not be tolerable; a ZERO will be given to any cheated assignment/exams, and it will be reported to the Department and the University.
- Do NOT share/post online any course materials, PPT slides, or homework solutions.
- Use of electronic devices during exams is NOT allowed unless stated otherwise.
- You are required to check Canvas for reading/assignments.
- The information on this syllabus is subject to change; changes, if any, will be clearly explained in class, and it is your responsibility to become aware of them.
- Once the class starts, use Canvas Inbox to email me for a faster response. I check the Canvas Inbox emails much more often than my school emails.

Class Format

- Course materials such as syllabus, handouts, notes, assignment instructions, etc. can be found on Canvas at <http://sjsu.instructure.com>.
- You are responsible for regularly checking the most updated messages and uploaded materials there.

Program Information

Diversity Statement - At SJSU, it is important to create a safe learning environment where we can explore, learn, and grow together. We strive to build a diverse, equitable, inclusive culture that values, encourages, and supports students from all backgrounds and experiences.

Course Goals

Introduction to the basic concepts of computer hardware structure and design, including processors and arithmetic logic units, pipelining, and memory hierarchy.

Course Learning Outcomes (CLOs)

Upon successful completion of this course, students will be able to:

- Understand the role of each major hardware component of a computer system and their synergistic interaction with each other and software.
- Analyze and perform tradeoffs between the cost, performance, and reliability of alternative computer architectures.
- Understand, analyze, and design digital logic structures for the basic combinational and sequential circuits.
- Understand the alternative binary internal representation of information (such as sign-magnitude, one's complement, two's complement, and floating point) along with their optimizations and tradeoffs.
- Be able to perform basic mathematical operations (add, multiply) in the various Boolean number representation schemes.
- Understand the operation of, and be able to analyze from a cost/performance standpoint, certain optimized hardware structures.
- Appreciate the need to use a memory hierarchy and understand how locality of memory referencing in typical programs can be leveraged to perform effective memory architecture management.
- Understand and emulate the various mapping, replacement, and dynamic memory allocation algorithms for cache and virtual memory management.
- Understand the rationale and philosophy behind both complex instruction set computers (CISC) and reduced instruction set computers (RISC), and the tradeoffs between the two architectures.
- Understand how pipelining and parallel processing are cost-effective methods of increasing hardware performance.

Course Materials

Computer Organization and Design – The Hardware/Software Interface, 5th

Author: David A. Patterson, John L. Hennessy

Publisher: Elsevier

Edition: 5th

ISBN: 9780124077263

Required Textbooks

Logic & Computer Design Fundamentals

Author: Mano & Kime

Publisher: PEARSON

Edition: 5th

ISBN: 9780131989269

Optional Textbooks

Course Requirements and Assignments

Assignments:

- No late assignments will be accepted without advanced arrangement with the instructor.
- At the end of the semester, two 24-hour late passes may be applied to two submissions that are not later than 24 hours.
- All homework must clearly indicate each student's name, course, and assignment number.
- Students are allowed (and actively encouraged) to form study groups.
- You may discuss solutions, but you **MUST** write up the answers independently.
- If you use a website or reference book, you must cite it.
- If there are multiple similar submissions not exhibiting independent thought, or with words obviously lifted from a book or website, ALL such submissions will receive scores of 0.

LockDown Browser + Webcam Requirement:

This course requires the use of LockDown Browser and a webcam for online quizzes. The webcam can be the type that's built into your computer or one that plugs in with a USB cable. Watch [this](#) brief video to get a basic understanding of LockDown browser and the webcam feature. Download and install LockDown browser from [here](#).

Pop Quizzes:

- Pop quizzes locked with passcode may be given anytime during class.
- They are usually explained in class and due on the end of the lecture day.
- The purpose of pop quizzes is to encourage you to study and review the concepts and materials we discussed in the lecture.

Midterm and Final Examinations:

There will be two midterm examinations, and a cumulative final exam.

- Exams may NOT be taken before or after the scheduled time for any reason.
- All the students need to attend synchronously.
- No make-up exams for anyone except for the medical emergency with the official medical proof.
- Use of electronic devices during exams is NOT allowed unless stated otherwise.
- All exams include quizzes (closed book) and written test (open book)
- All exams will remain with the instructor.

Grading Information

- Final grades will not be adjusted in any way - so an 89.99% is still a B+.
- No incomplete grades will be given.
- The grading scale is as follows:
- Note that "All students have the right, within a reasonable time, to know their academic scores, to review their grade- dependent work, and to be provided with explanations for the determination of their course grades."

- ee University Policy F13-1 at <http://www.sjsu.edu/senate/docs/F13-1.pdf> for more details.

Breakdown

- Participation 5%
- Pop quizzes 15%
- Homework 15%
- Project 15%
- Midterm 1 15%
- Midterm 2 15%
- Final Exam 20%

Criteria

The grading scale is as follows:

Grading Scale					
A+	97%	A	93%	A-	90%
B+	87%	B	83%	B-	80%
C+	77%	C	73%	C-	70%
D+	67%	D	63%	D-	60%
F	below 60.0%				

University Policies

Per [University Policy S16-9 \(PDF\)](http://www.sjsu.edu/senate/docs/S16-9.pdf) (<http://www.sjsu.edu/senate/docs/S16-9.pdf>), relevant university policy concerning all courses, such as student responsibilities, academic integrity, accommodations, dropping and adding, consent for recording of class, etc. and available student services (e.g. learning assistance, counseling, and other resources) are listed on the [Syllabus Information](https://www.sjsu.edu/curriculum/courses/syllabus-info.php) (<https://www.sjsu.edu/curriculum/courses/syllabus-info.php>) web page. Make sure to visit this page to review and be aware of these university policies and resources.

Course Schedule

Course Schedule (This schedule is subject to change. Any change will be communicated via Canvas with fair notice.)

Week	Date	Topics, Readings, Assignments, Deadlines
1	8/22,8/24	Introduction, Logic Design
2	8/29,8/31	Logic Design

3	9/5, 9/7	Logic Design , MIPS Instructions
4	9/12, 9/14	MIPS Instructions
5	9/19, 9/21	MIPS Instructions
6	9/26,9/28	MIPS Instructions, Arithmetic
7	10/03, 10/05	Arithmetic for Computers, Midterm 1
8	10/10, 10/12	Arithmetic for Computers
9	10/17, 10/19	The Processor
10	10/24,10/26	The Processor
11	10/31-11/2	Memory Hierarchy
12	11/7, 11/9	Review, Midterm 2
13	11/14, 11/16	Memory Hierarchy
14	11/21, 11/23	Memory Hierarchy
15	11/28, 11/30	Memory Hierarchy, Thanksgiving Holiday
16	12/5	Virtual Memory
Final Exam	12/14	Thursday, 12:15-2:30 PM <div style="border: 1px solid black; height: 20px; width: 100%; margin-top: 5px;"></div>