IBM SYNAPSE MIMICS HUMAN BRAIN

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ABSTRACT

Nowadays, without computers we can't perform any task. Many big tasks are being performed easily and this is made possible through Micro Processors. Due to increase in demand to build computers with high performance and low power consumption, new ways are being explored. IBM's SYNAPSE chip is one of the results of such exploration. SYNAPSE has a brain-inspired computer architecture powered by unprecedented 1 million neurons. This chip is largest chip built by IBM till date with high performance and low power consumption. This chip project is called DARPA SYNAPSE program and the main collaborators are IBM, HP and HRL. This paper mainly covers the following.

1. Evolution of Micro Processors
2. Features of Brain
3. Background
4. Project Phases of DARPA SyNAPSE
5. Results
6. Collaborators

1. INTRODUCTION

The force that drives the computer mainly is the micro-processor and it is thing which performs many tasks and gives the output accordingly. From the dawn of the micro-processors continuous research and innovation is going on how to increase the performance of it by increasing the computing power and having less power consumption. Many companies have come up with different solutions like AMD series Processors by AMD, Pentium series by INTEL, Power series by IBM etc. But still there is some lagging in the Processor performance. To full fill this, one approach which is carried out is to mimic the mammalian brain to build a microprocessor system through DARPA SyNAPSE Program.

SyNAPSE is a DARPA-funded program to develop electronic neuromorphic machine technology that reaches to biological levels. In a simple definition, it is an attempt to build a new kind of computer with similar form and function to the mammalian brain. Such artificial brains which are created would be used to build robots whose intelligence matches that of cats and mice. SyNAPSE stands for Systems of Neuromorphic Adaptive Plastic Scalable Electronics. It started in 2008 and as of January 2013 has received $102.6 million funding. It is scheduled to run until around till 2016 and get impressive results. The project is primarily contracted to IBM, HP and HRL who in turn subcontracted parts of the research to various US universities. The ultimate aim is to build an microprocessor system that matches a mammalian brain in function and power consumption. It should recreate 10 billion neurons, 100 trillion synapses, consume one kilowatt [1]

2. EVOLUTION OF MICROPROCESSORS

The first microprocessor was introduced in the year 1968 by the INTEL Corporation. It was a 4 bit processor named 'Intel 4004' and it performs logical operations like addition, subtraction. Later the 8 bit chips were introduced which perform logical operations using 8 bit words. Many processors have been introduced later as predicted by Moore's law. The law states that the number of transistors on integrated circuits double every 18 months. His prediction has been come true for almost 50 years.

2.1 16 - Bit Chips

In the middle of 1970s, National Semiconductor entered microprocessors field development, enticed by the fast pace of breakthroughs and development at Intel. Unfortunately, the era of 16-bit chips ended early; even by the standards of such an industry.16-bit microprocessors including National Semiconductor's PACE microprocessors were relatively slow. By the time 16-bit chips were living up to their expectations, the 32-bit era had already begun to arrive and 16-bit technology faded slowly [12].

2.2 32 - Bit Chips

By the late 1970s, development of 32-bit microprocessors was in full sound and they began to appear on the market in the 1980s, courtesy of National Semiconductor and HP. Desktop engineering devices entered a revolutionary phase with the dawn of 32-bit processing. 32-bit microprocessors were relatively advanced and perform many complex operations easily [12].

2.3 64 - Bit Chips

64-bit chips have been available in the market since 1992, and are now used in most of computers. Much of the 64-bit microprocessor era has been the battle between Intel and AMD. The latter company AMD was founded in 1969 and rose to prominence after making a deal with IBM and Intel through which AMD would become the second source manufacturer of Intel-designed processors. From that agreement, as prompted by IBM's internal policies at the time, was born a legal controversy and ultimately the development of a micro processing market with two major superpowers [12] .

2.3 RISC Chips

RISC which is defined as Reduced Instruction Set Computer derived from an IBM research project dating back to the second half of the 1970s. RISC chips operate by omitting the complex instructions and relying more effectively on the simpler, more common instructions that could be processed and acted upon more quickly. Such chips are still used today and have become into a spectrum of fully fledged computing architectures in competition with CISC, which uses complex instructions. RISC architecture is used widely in devices like cellular phones and certain types of mobile PCs [12].

In this manner the development of chips have been advanced and many processors are available in which perform very complex operations. But the processors are tied with many constraints like high power consumption for increasing the computing power etc. So many thought that replication of brain architecture of mammal would be a good choice which can solve many problems of the present microprocessors. This is made possible through DARPA SyNAPSE program. Initially IBM released a chip in 2011 with one core and 256 neurons and now in 2014 they have released a chip, which can be powered with a hearing aid battery that contains 5.4 billion transistors, 4096 neurosynaptic cores, one million programmable spiking neurons and 256 configurable synapses and consumes very little power about $1/10^{th}$ of a megawatt.

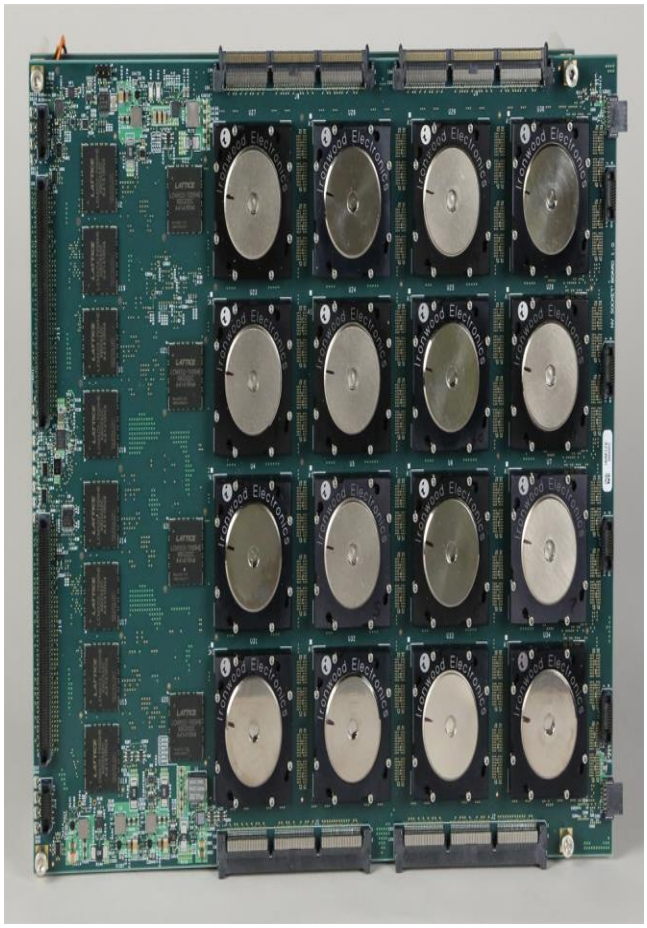

Figure 1: IBM's 4x4 array of SyNAPSE chips each one with 1 million electronic neurons and 256 million electrical synapses between them [7]

The following section is a description of brain features which would give a good idea of why we can consider brain architecture to develop an electronic microprocessor system.

3. FEATURES OF BRAIN

A human brain almost consists of about 1 billion neurons. A neuron is an electrically excitable cell that processes and transmits information through electrical and chemical signals. The signals which occur between the neurons occur mainly through Synapses which are specialized connections with the other cells. These neurons can connect to each other and they form neural networks. The neurons can process the information very fast and can transmit them also in a very fast way. Through this type of network we can almost process any amount of information and take decisions in a right manner. But now we are using only about 10% of the brain and through this only we can achieve many things. If we can make this architecture apply to the microprocessor system then we can almost achieve wonders by making only a percentage it becoming applicable. In the present processors computation is constrained by power and speed. There is Von Neumann bottleneck problem where the chip cannot feed the data in the memory to the processing core fast enough. By using this brain mimic architecture we can overcome this computation problem [11].

4. BACKGROUND

Over a period of six decades, modern electronics has evolved through a series of major advancements leading to the programmable electronic machines that we use today. Due to limitations in hardware and architecture, these machines are of limited utility in complex real-world environments, which demand an intelligence that has not yet been captured in an algorithmic-computational paradigm. The SyNAPSE program seeks to break this programmable machine paradigm and lay a new path forward for creating useful and intelligent machines. The vision for the DARPA SyNAPSE program is the enabling of electronic neuromorphic machine technology that is scalable to different biological levels. Programmable machines are limited by their computational capacity and also by an architecture requiring human-derived algorithms to describe and process information from their environment. In contrast, biological neural systems autonomously process information in very complex environments by automatically learning similar and probabilistically stable features and associations. The key to achieving the vision of the SyNAPSE program will be an approach that can coordinate aggressive technology development activities in the following areas [5].

4.1 HARDWARE - implementation will likely include novel synaptic components, CMOS devices and combinations of hard-wired and programmable/virtual connectivity. These will support critical information processing techniques observed in biological systems, such as spike timing dependent plasticity and spike encoding.

4.2 ARCHITECTURE - will support important and critical structures and functions observed in biological systems such as core component circuitry, connectivity, hierarchical organization, competitive self-organization and

modulatory/reinforcement systems. In biological systems, processing will be maximally nonlinear, distributed and inherently noise- and defect-tolerant.

4.3 SIMULATION – It requires large-scale digital simulations of circuits and systems will be used to prove component and whole system functionality and to inform overall development of the system in advance of neuromorphic hardware implementation.

4.4 ENVIRONMENT – It involves virtual platforms for the training, evolving, evaluation and benchmarking of intelligent machines in various aspects of cognition, perception and response.

This ambitious goal will require the collaboration of numerous disciplines such as large-scale computation, neuromorphic VLSI, information science, cognitive science, computational neuroscience, artificial neural networks, unconventional nanometer-scale electronics, and CMOS design and fabrication.

5. PROJECT PHASES OF DARPA SYNAPSE

The following are the phases in the project and it is made clear that no phase should last more than 18 months. The targets may vary between depending on the outcome of the previous stages.

5.1 PHASE 0

This phase included feasibility study for over a period of 9 months. The aim is demonstrate an electronic synaptic component exhibiting Spike-Timing dependent Plasticity (STDP) with a specified set of parameters. In here the chosen microcircuits must support the larger system architecture and demonstrate spike time encoding, spike time dependent plasticity and competitive neural dynamics [1].

5.1 PHASE 1

In this phase chip fabrication process supporting the architecture with 10bn synapse per square centimeter and 1million neurons for square centimeter is specified. A neuromorphic design methodology that can specify all components, connectivity, subsystems of a complete system. Electronic implementation, simulation and environment are decided here and the work is carried accordingly [1].

5.1 PHASE 2

In this phase designing a complete neural system, a single chip neural system, expanding a sensory and navigation environment is taken care of over here. The simulation testing is carried out to check the responses between the synapses to identify the faults and rectify them accordingly.

5.1 PHASE 3

This is carried out for about a period of 1 year between late 2012 and 2013. In here a single chip neural system is completely developed and simulation testing is carried out. A symbolic and sensory environment is added over here.

5.1 PHASE 4

In this phase the fabrication of 100 million neurons is carried out. This is installed in a cat level robot and this is yet to be carried out and is in development. With this step we can say that a major milestone has been achieved.

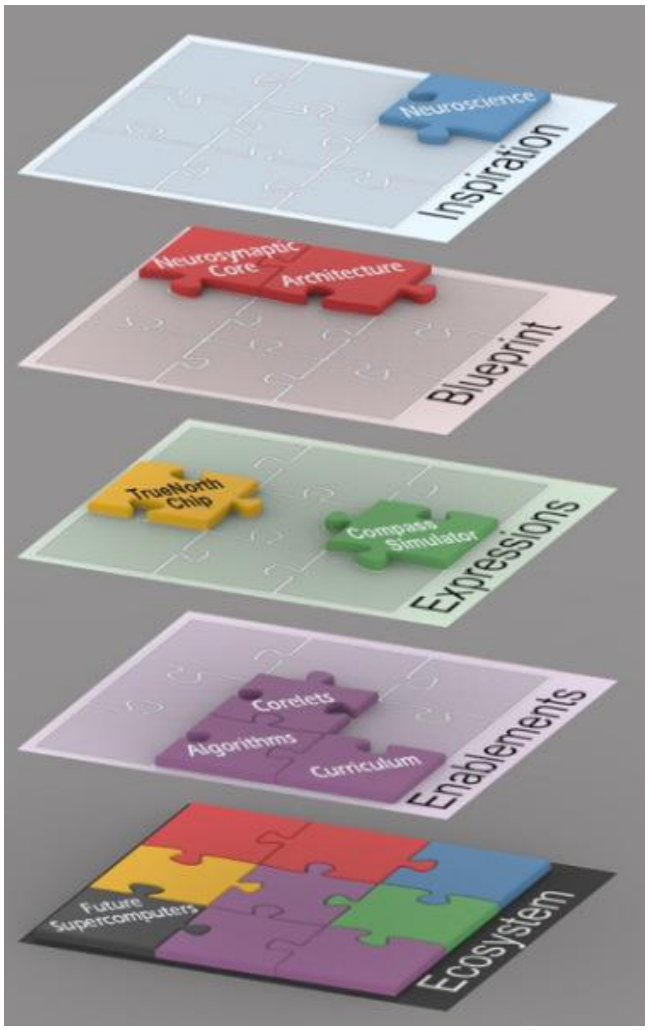

FIGURE 2: IBM SyNAPSE ARCHITECTURE [4]

6. RESULTS

The following are the results that are obtained from work from different phases:

6.1 CAT-SCALE BRAIN SIMULATION

IBM developed a massively parallel cortical simulator called C2. It ran on the Blue Gene/P supercomputer named Dawn. The largest cortical simulation consisted of 1.6 billion neurons and 8.87 trillion synapses. This matches the scale of that of a cat cortex and 4.5% the scale of a human cortex. The simulation ran at 643 times slower than real time. The simulations incorporated STDP, single-compartment spiking neurons and axonal delays. The simulation time step was 0.1 milliseconds. The architecture and connectivity of the simulated network was biologically inspired. It included attendant sections of the thalamus, the visual cortex and the reticular nucleus. Regions of the simulated cortex were constructed from thalamocortical modules. Each module had 334 thalamic neurons, 10,000 cortical neurons and 130 reticular

nucleus neurons. Within each module the cortical neurons were further subdivided into 4 layers (real mammalian brains have six layers).The largest model had 278 x 278 modules making a total of 1.6 billion neurons. The SpikeStream was a framework to supply sensory stimulus information which is encoded in spikes. The spikes were encoded to represent auditory utterances of the alphabet geometric visual objects and [1].

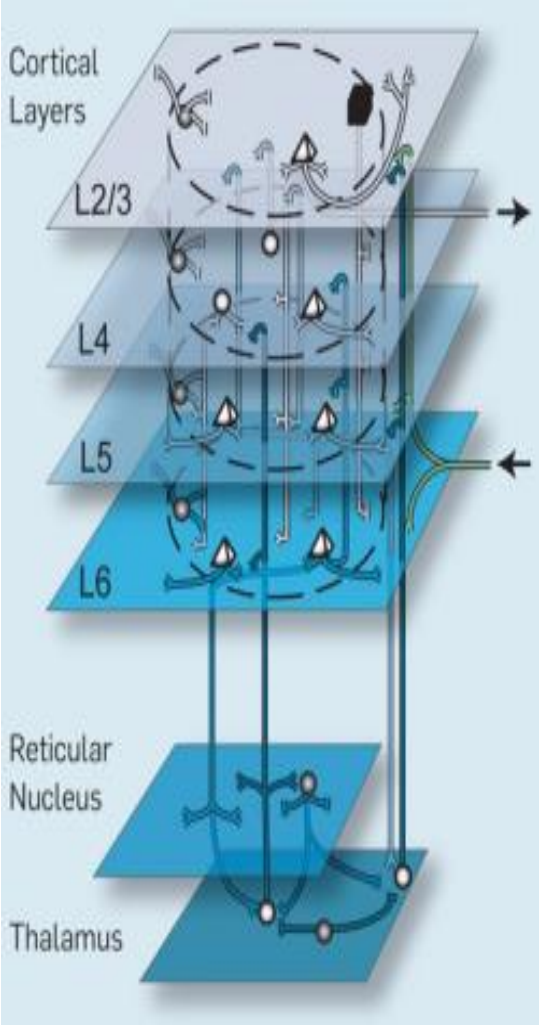

FIGURE 3: Cortical model used in simulations [1]

6.2 DIGITAL NEUROSYNAPTIC CORE

In August 2011 IBM had announced that they had built a digital neurosynaptic core. The microprocessor implements 256 leaky integrate-and-fire neurons in CMOS hardware. The neurons are arranged in a 16x16 array. Each neuron is connected to others by 1,024 synapses, making a total of 262,144 synapses per core. The newest laptops ship with 22 nm processors as of August 2012. The entire core has 3.8 million transistors and fits inside 4.2 mm^2. Each neuron occupies 35 µm x 95 µm Compare this to a real neuron body which is about 4 to 100 µm in diameter. The core was mounted on a custom-built printed circuit board and connected to a personal computer via USB. This way it could be interfaced to various virtual and real environments. The core learned to recognize handwritten digits and could also play a game of pong [1].

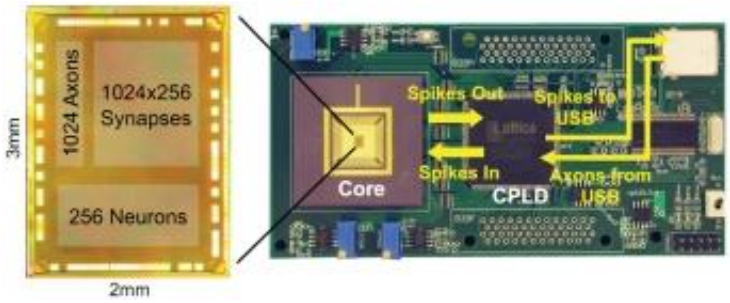

FIGURE 4: Neurosynaptic core and Board [1]

6.3 THE IBM BRAIN WALL

The "brain wall", pictured below, is a visualization tool built by IBM at their Almaden research center in California. It allows researchers to see the overview of neuron activation states in a large-scale neural network. Patterns of neural activity are observed as they move across the network. The 4x4 array of flat-screen monitors can display about 262,144 neurons simultaneously. Each neuron is represented by one grey pixel each. Larger networks might be visualized in future by grouping multiple neurons per pixel. The tool can be used to visualize activity within a neurosynaptic core as well as supercomputer simulations.

FIGURE 5: IBM Brain wall [1]

6.4 MEMORISTOR CHIP

HRL Labs announced in December 2011 that they have built a memristor array which is integrated on top of a CMOS chip. This was the first ever functioning demonstration of a memristor array. Due to the low power requirements and high circuit density, memristor technology is considered important for the continuation of Moore's Law. The HRL chip has a multi-bit fully-addressable memory storage capability with a density which is up to 30 Gbits/cm^2. Such density is unprecedented in microelectronics. The logic processing capability of memristors and simultaneous memory storage makes them very suitable for neuromorphic computing. The logic and memory units are one and the same, much like the neural circuits of the brain. HRL's hybrid crossbar/CMOS system can reliably store 1,600 pixel images using a new programming scheme. Ultimately the team plans to scale the chip to support emulation of millions of neurons and billions of synapses. In the future it is possible that this memristor technology can be used to implement variants of the neurosynaptic core is described above. By using memristors, these cores could be reduced in energy consumption and size, thus making it more practical to build very large arrays of cores with enough numbers of neurons to match the human brain [1].

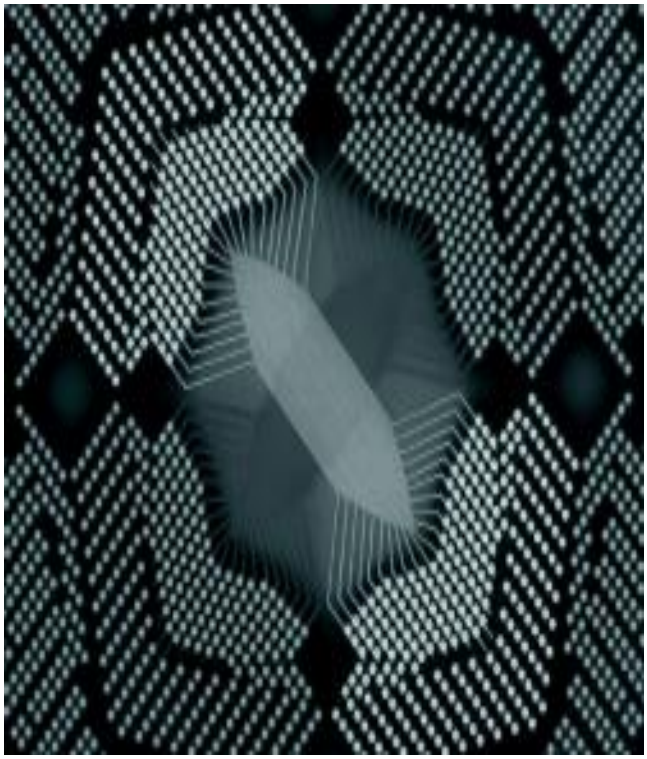

FIGURE 6: Memoristor Cross Bar array [1]

6.5 NEUROMORPHIC ARCHITECTURE

This neuromorphic architecture (pictured right) contains 766 spiking artificial neurons arranged in layers format much like the hierarchy found in the human brain. Although it uses simple leaky integrate-and-fire (LIF) neurons and simple binary synapses, it is nevertheless capable of motion detection, robust visual object recognition and motor control outputs. This has been proven by testing the network in simulation on a standard computer. The network utilizes synaptic homeostatic renormalization and burst-STDP - two relatively new ideas in the field of spiking neural networks. The architecture has been designed with a view to deploying it on the digital neurosynaptic cores which are described above. IBM is currently working on inter-core communication to build a large on-chip network of these cores. The 766-neuron circuit is only a "minimum framework" prototype. It is expected to be scaled up to thousands or hundreds-of-thousands of neurons as the hardware becomes efficient and available.

6.6 TRUENORTH AND COMPASS

TrueNorth is a scalable, novel modular, non-von Neumann, cognitive computing, ultra-low power architecture being developed by IBM as part of the SyNAPSE program. It consists of a scalable network of neurosynaptic cores with every core containing dendrites, neurons, axons and synapses.

Compass, also developed by IBM, is software which simulates the TrueNorth architecture. It enables testing of the architecture on a mainstream supercomputer before building directly in specialized neuromorphic hardware. Besides being a massively-parallel functional simulator, multi-threaded, Compass is also a parallel compiler that can map a network of long-distance neural pathways in the macaque monkey brain to TrueNorth [1].

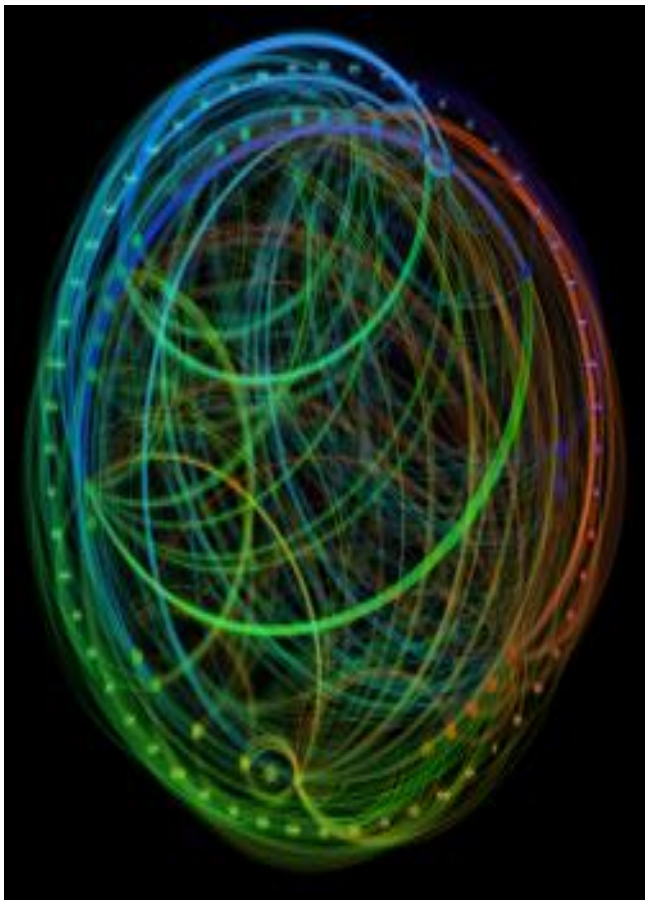

FIGURE 7: Neural Pathways of a macaque monkey brain simulated in the TrueNorth architecture [1]

7. COLLOBARATORS

IBM and HRL are the main contractors in the DARPA SyNAPSE program and they have sub contracted some work to universities. Some of them are Cornell University, University of California-Merced, University of Wisconsin- Madison, Boston University, Portland State University, Stanford University, University of California-Irvine, and University of Michigan etc.

8. CONCLUSION

In the ways of exploration to find a better microprocessor we have definitely moved forward through this program. IBM has released the world's first neurosynaptic computer chip which mimics the brain computing abilities and power efficiency known as TrueNorth. It is one of the most powerful and efficient chips in the history of computing. It utilizes only 70 mill watts of power to perform complex tasks. We have moved beyond the Von Neumann bottleneck also. But we are mimicking the brain up to a little percentage only. Research is still going on to find out how can we build a processor that mimics the brain with its whole capacity. Hopefully we can see the microprocessors in the near future which can function like a human brain with full capacity.

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