Ahmet Bindal

EDUCATION

June 1988 **Ph.D. in Electrical Engineering**, University of California, School of Engineering and Applied Science, Los Angeles, California.

June 1982 **M.S. in Electrical Engineering**, University of California, School of Engineering and Applied Science, Los Angeles, California.

June 1978 **B.S. in Electrical Engineering**, Bogazici University, Electrical Engineering Department, Istanbul, Turkey.

PROFESSIONAL EXPERIENCE

San Jose State University, Computer Engineering Department
9/02 – Present –*Professor*
Teaching assignments include Computer Design and Architecture and Digital Electronics.

Research area concentrates on designing ultra-low power surrounding-gate silicon nanowire transistors for the next generation nano- circuits and architectures.

Tality Corporation
1/00 – 9/02 – *Senior Chip Architect*
Developed architectural specifications of a System On Chip (SOC) design for 802.11b Wireless Local Area Network (WLAN). In this design, AMBA 2.0 bus is used to interface with the ARM 9 core, SRAM, SDRAM, various serial peripheral devices and the Direct Memory Access (DMA) engine, which maintains data transfers between a Base-Band, Spread Spectrum Modem and the memory subsystems.

Involved in the development of a Base-Band, Spread Spectrum transmitter. Designed the BCH Encoder, QPSK/8PSK modulator, Spreader and the Super Frame Timing units.

Cadence Design Systems, Design Services Division
3/98 – 1/00 - *Senior Technology Architect*
Developed interface between a 32-bit socketizable MIPS processor and ARM 7 processor's AMBA bus for fully integrated embedded platforms.

Studied various aspects of Signal Integrity issues on VLSI systems with emphasis on cross-coupling. Developed design guidelines to prevent cross-coupling related glitches and parasitic delays.

Studied architectural and micro-architectural aspects of a Data Driven Multimedia Processor (DDMP). Designed asynchronous clock methodologies for this processor

using c-elements. The c-element is also improved to eliminate its state dependent instabilities.

Philips Semiconductors, VLSI division
8/95 – 3/98 *Trimedia group – Member of Technical Staff*
Redesigned data and instruction caches, register file and various generic SRAM buffers in TM1 chip using 0.35 um process. Repeated the same tasks for TM1C (compacted) chip using 0.25 um process.

Micro-architected the Video Out unit in TM1 chip. The unit performed 4:2:2 or 4:2:0 interspersed-cosited transformations, horizontal upscaling and alpha-blending using YUV image format with and without overlay. Also verified the Video Out unit by programming its control and memory interface registers.

Designed a clock tree for TM1 chip using 0.5 um technology. The worst case clock skew on the tree was 100 ps and clock rise/fall time was under 500 ps with varying load conditions.

Intel Corporation, Microprocessor Division
6/94 – 8/95 *P6C MMX Unit – Senior Circuit Design Engineer*
Designed a fully-custom 16-bit signed static CMOS multiplier for the MMX unit using 0.25 um technology with a 2.5 V power supply. The multiplier executes its task within 3 clock cycles at 250 MHz and it occupies approximately 600 um by 600 um area.

IBM Business Systems Division
1/93 – 6/94 *System Hardware Development – Staff Engineer*
Designed a fully-custom 64-bit domino CMOS carry-select, carry-look-ahead adder for an integer point processor using 0.25 um technology with 2.5 V power supply. Circuit simulations on the critical path showed 1.55 ns evaluate time and 0.5 ns precharge time.

Formulated the distributed area, coupling and fringing capacitance, in-line and mutual inductance of on-chip interconnect wires with varying geometry using MAXWELL analysis tool.

IBM General Technology Division
10/88 – 1/93 *Semiconductor Research and Development – Staff Engineer*
Designed a 0.1 um nMOS transistor using 1.5 V power supply for high speed, low power applications. The stand-by current of the device was 1 nA/um and oxide thickness was 50 A.

Designed 0.25 um nMOS/pMOS transistors using both 2.5 V and 3.3 V power supply voltages for a 256 Mbit DRAM project. The stand-by current was 1 pA/um and oxide thickness was 70 A.

Developed and designed the entire process flow for fabricating symmetrical, self-aligned, gate-overlapped-drain nMOS/pMOS transistors using Sidewall Image Transfer (SIT) technology.

Designed a novel process flow for a fully-depleted SOIFET technology using sidewall-less Si3N4 and SiO2 chemical/mechanical polish stop layers. The SOI layer was 500 A (+/- 100 A) across 5 inch wafer.

HUGHES AIRCRAFT Semiconductor Division
9/82 – 6/88 *Semiconductor Research and Development – Researcher*
Conducted research in the area of silicon ion implantation in undoped, LEC-grown GaAs. The emphasis was on determining the activation efficiency of Si using Secondary Ion Mass Spectroscopy (SIMS), conventional and step-etch C-V techniques.
Investigated shallow and deep level defect centers of LEC-grown GaAs using Photoluminescence and Deep Level Transient Spectroscopy (DLTS), respectively.

MONOGRAM INDUSTRIES
9/80 – 6/82 *Solar Cell Researcher*
Characterized thermally evaoparted CdS and CdTe polycrystalline thin film semiconductors for solar cell applications. Designed 18% efficient CdS-CdTe solar cells for space applications.

PUBLICATION LIST

(1) A. Bindal, D. Wickramaratne, S. Hamedi-Hagh, "Implementation of a Direct Sequence Spread Spectrum Baseband Transmitter Using Silicon Nanowire Technology", J. of Nanoelectronics and Optoelectronics, Vol. 5, No. 1, p. 1-12, 2010.

(2) A. Bindal, T. Ogura, N. Ogura, S. Hamedi-Hagh "Silicon Nanowire Transistors for Implementing a Field Programmable Gate Array Architecture with Scan Chain", J. of Nanoelectronics and Optoelectronics, Vol. 4, No. 3, p. 342-352, 2009.

(3) S. Hamedi-Hagh and A. Bindal, "Design and Characterization of the Next Generation Nanowire Amplifiers", VLSI Design, Vol. 2008, Article ID: 190315, 2008.

(4) S. Hamedi-Hagh, A. Bindal "Spice Modeling of Silicon Nanowire Field-Effect Transistors for High-Speed Analog Integrated Circuits", IEEE Trans. Nanotechnology, Vol. 7, No. 6, p. 766-775, 2008.

(5) A. Bindal, S. Hamedi-Hagh, T. Ogura, "Silicon Nanowire Technology for Applications in the Field Programmable Gate Array Architectures", J. of Nanoelectronics and Optoelectronics, Vol. 3, p. 113-122, 2008.

(6) S. Hamedi-Hagh, A. Bindal, “Characterization of Nanowire CMOS Amplifiers Using Fully Depleted Surrounding Gate Transistors”, J. of Nanoelectronics and Optoelectronics, Vol. 3, p. 1-8, 2008.

(7) A. Bindal, D. Wickramarathe, S. Hamedi-Hagh, T. Ogura, “An FPGA Architecture Using Vertical Silicon Nanowire Transistors”, Proc. of Nano Sci. and Technol. Inst. (NSTI), Boston, Massachusetts, 2008.

(8) A. Bindal, S. Hamedi-Hagh, “An Exploratory Design Study of a 16x16 Static Random Access Memory Using Silicon Nanowire Transistors”, J. of Nanoelectronics and Optoelectronics, Vol. 2, p. 294-303, 2007.

(9) A. Bindal, A. Naresh, P. Yuan, K. K. Nguyen, S. Hamedi-Hagh, “The Design of Dual Work Function CMOS Transistors and Circuits Using Silicon Nano Wire Transistors”, IEEE Trans. Nanotechnology, Vol. 6, No. 3, p. 291-302, 2007.

(10) A. Bindal, S. Hamedi-Hagh, “The Design of a Dual Work Function Spiking Neuron Using Silicon Nano-Wire Technology”, Nanotechnology (Institute of Physics), Vol. 18, 095201, 2007.

(11) A. Bindal, S. Hamedi-Hagh, “Static NMOS Circuits Using Silicon Nano-Wire Technology for Crossbar Architectures”, Semicond. Sci. Technol. (Institute of Physics), Vol. 22, p. 54-64, 2007.

(12) A. Bindal, S. Hamedi-Hagh, “An Exploratory Study on Power Efficent Silicon Nano-Wire Dynamic NMOSFET/PMESFET Logic”, IET (formerly IEE) Sci. Meas. Technol. Vol. 1, No. 2, p. 121-130, 2007.

(13) A. Bindal, S. Hamedi-Hagh, “An Integrate and Fire Spiking Neuron Using Silicon Nano-Wire Technology”, Proc. of Nano Sci. and Technol. Inst. (NSTI), San Jose, California, 2007.

(14) A. Bindal, S. Hamedi-Hagh, “The Impact of Silicon Nano-Wire Technology on the Design of Single Work Function CMOS Transistors and Circuits”, Nanotechnology (Institute of Physics), Vol. 17, p. 4340-4351, 2006.

(15) A. Bindal, S. Hamedi-Hagh, “The Design and Analysis of Dynamic NMOSFET/PMESFET Logic Using Silicon Nano-Wire Technology”, Semicond. Sci. Technol. (Institute of Physics), Vol. 21, p. 1002-1012, 2006.

(16) A. Bindal, B. Gordon, A. Reynolds, A. Salsbery, B. Wang, “A Data-Flow Platform for Implementing Algorithm-Dependent ASIC Hardware Using Data-Driven Processors”, Int. Conf. Digital Telecomm. (ICDT), Cap Esterel, France, 2006.

(17) A. Bindal, K. Aflatooni, “The Design of a Silicon Wire DRAM Cell for Very Dense DRAM Architectures”, Proc. of Nano Sci. and Technol. Inst. (NSTI), Anaheim, California, 2005.

(18) A. Bindal, S. Mann, B. Ahmed, L. Raimundo, “An Undergraduate System-On-Chip Course for Computer Engineering Students”, IEEE Trans. Education, Vol. 48, No. 2, p. 279-289, 2005.

(19) A. Bindal, S. Jit, A. Simpson, “The Design of Autonomous Mobile Predator and Prey Robots”, Int. Conf. Comput. Intel. Multi. Apps. (ICCIMA), Las Vegas, Nevada, 2005.

(20) A. Bindal, S. Brugada, T. Ha, W. Sana, M. Singh, V. Tejaswi, and D. Wyland, “A Simple Micro-Threaded Data-Driven Processor”, IEEE Euromicro Symp. Digital Sys. Des., Rennes, France, 2004.

(21) A. Bindal, D. Parent, L. He, S. Kilic, “A MOSFET Design Laboratory”, Int. Conf. Eng. Edu., Gainesville, Florida, 2004.

(22) A. Bindal, S. Mann “A System-On-Chip Course Using Altera’s Excalibur Device and Quartus II Software”, Int. Conf. Eng. Edu., Gainesville, Florida, 2004.

(23) A. Bindal, N. Rovedo, J. Restivo, C. Galli, S. Ogura, “Fabrication of Extremely Thin Silicon on Insulator for Fully-Depleted CMOS Applications”, Thin Solid Films, 1993, p. 105.

(24) A. Bindal, K. L. Wang, S. J. Chang, O. M. Stafsudd, “Major Implantation-Induced Defects in Conventional and Rapid Annealed, Silicon Implanted LEC-Grown GaAs”, J. Electrochemical Soc., Vol. 138, No. 1, 1991, p. 222.

(25) A. Bindal, R. Wachnik, W. Ma, “Observation of Recombination Center-Assisted Tunneling Current in Al(Cu)-Penetrated PtSi Schottky Barrier Diodes”, J. Appl. Phys. Vol. 68, No. 12, 1990, p. 6259.

(26) A. Bindal, K. L. Wang, S. J. Chang, M. A. Kallel, “On the Nature of the Silicon Activation Efficiency in Liquid-Encapsulated Czochralski-Grown GaAs by Photoluminescence”, J. Appl. Phys, Vol. 65, No. 3, 1989, p. 1246.

(27) A. Bindal, K. L. Wang, S. J. Chang, M. A. Kallel, P. K. Chu, “A Process Simulation Model for Silicon Ion Implantation in Undoped, LEC-Grown GaAs”, J. Electrochemical Soc., Vol. 136, No. 8, 1989, p. 2414.

BOOKS

(1) Ahmet Bindal, “Fundamentals of Computer Architecture and Design” accepted by Springer for publication, Dec. 30, 2014.

(2) Ahmet Bindal, “Electronics for Embedded Systems” accepted by Springer for publication.

(3) Ahmet Bindal, Sotoudeh Hamedi-Hagh, “Silicon Nanowire Transistors: Design and Applications”, to be submitted to Springer for publication.

(4) Salih Kilic, Ahmet Bindal, “An NMOS Transistor with Localized Channel and Pocket Implantation”, Lambert.

PATENT/DISCLOSURE LIST

(1) A. Bindal, “Sidewall Lithography for Growing Horizontal Carbon Nano Tubes and a Process Flow for Complementary Carbon Nano Tube Field Effect Transistor (CCFET) Fabrication”, provisional patent application, Oct. 2003, serial no: 60/512,137.

(2) A. Bindal, “A Self-Assisted Lithography for Manufacturing Nano-Interconnects and Catalyst Islands for Growing Carbon Nano Tubes”, provisional patent application, Oct. 2003, serial no: 60/510,276.

(3) A. Peleg, M. Mittal, L. Mennemeier, B. Eitan, C. Dulong, E. Kowashi, W. Witt, D. Lin, A. Bindal, “An Apparatus For Performing Multiply-Add Operations on Packed Data”, Feb. 1996, No. 6,035,316.

(4) A. Bindal, “MOS Channel Device with Counterdoping of Ion Implant for Reduced Substrate Sensitivity”, Aug. 1996, No. 5,548,148.

(5) A. Bindal, C. Galli, N. Rovedo, “Thin SOI Layer for Fully Depleted Field Effect Transistors”, Nov. 1993, No. 5,264,395.

(6) A. Bindal, J. Currie, “Nitride Polish Stop for Forming SOI Wafers”, Nov. 1993, No. 5,262,346.

(7) A. Bindal, S. Ogura, “A Symmetrical FET Structure Using Reverse Sidewall Image Transfer Technique for CMOS6x (Leff = 0.1 to 0.15 um)”, Dec. 1991, Disclosure No: FI8-91-0850.

(8) A. Bindal, S. Ogura, “Self-Aligned, Double-gated, Fully-depleted SOI FET with 500 A Body Thickness”, Dec. 1991, Disclosure No: FI8-92-0008.

(9) A. Bindal, C. Galli, S. Ogura, “Sub-quarter micron Asymmetrical FET Using Sidewall Image Transfer (SIT) Technology”, Feb. 1992, Disclosure No: FI8-91-0607.